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Preparation and Characterization of Solution-Processed Nanocrystalline *p*-Type CuAlO₂ Thin-Film Transistors

Shuang Li, Xinan Zhang , Penglin Zhang, Xianwen Sun, Haiwu Zheng and Weifeng Zhang

Abstract

The development of p-type metal oxide thin-film transistors (TFTs) is far behind the n-type counterparts. Here, p-type CuAlO $_2$ thin films were deposited by spin coating and annealed in nitrogen atmosphere at different temperature. The effect of post-annealing temperature on the microstructure, chemical compositions, morphology, and optical properties of the thin films was investigated systematically. The phase conversion from a mixture of CuAl $_2$ O $_4$ and CuO to nanocrystalline CuAlO $_2$ was achieved when annealing temperature was higher than 900 °C, as well as the transmittance, optical energy band gap, grain size, and surface roughness of the films increase with the increase of annealing temperature. Next, bottom-gate p-type TFTs with CuAlO $_2$ channel layer were fabricated on SiO $_2$ /Si substrate. It was found that the TFT performance was strongly dependent on the physical properties and the chemical composition of channel layer. The optimized nanocrystalline CuAlO $_2$ TFT exhibits a threshold voltage of -1.3 V, a mobility of ~ 0.1 cm 2 V $^{-1}$ s $^{-1}$, and a current on/off ratio of $\sim 10^3$. This report on solution-processed p-type CuAlO $_2$ TFTs represents a significant progress towards low-cost complementary metal oxide semiconductor logic circuits.

Keywords: Solution-processed, p-type thin-film transistor, Nanocrystalline films, Mobility

Background

Over the past decades, metal oxide thin-film transistors (TFTs) have been extensively investigated for the next-generation active-matrix liquid crystal displays, organic light-emitting diode displays, and other emerging electronic circuits applications due to their excellent electrical properties and outstanding optical transparency [1, 2]. However, a majority of the metal oxide TFTs reported to date were focused on *n*-type materials [3]. The p-type oxide semiconductors are usually characterized with localized oxygen 2p orbitals with large electronegativity, self-compensation from oxygen vacancies, and the incorporation of hydrogen as an unintentional donor. Therefore, it is difficult in achieving effective hole doping [4]. Up to now, only a few p-type oxide materials (Cu₂O, CuO, SnO, etc.) were proved to be suitable for TFT application [5, 6], but their performance lags far behind of *n*-type counterparts. This limits the development of all oxide p-n junctions and complementary metal oxide semiconductor (CMOS) logic circuits.

To obtain a good p-type metal oxide, it is critical to modify the energy band structure and reduce the Coulomb force exerted by the oxygen ions on holes. thus motivating the discovery of a group of p-type delafossite oxides, such as CuMO₂ (M=Al, Ga, In) and SrCu₂O₂ [7, 8]. Among them, CuAlO₂ has a wide bandgap of ~ 3.5 eV, and its valence band maximums are dominated by a large hybridization of the oxygen orbitals with 3d¹⁰ electrons in the Cu1+ closed shell, which leads to a dispersive valence band. Meanwhile, the cations with closed shells (d¹⁰s⁰) are beneficial to achieve high optical transparency because such an electronic structure can avoid light absorption from the so-called d-d transitions. Therefore, it has attracted considerable attention since the first fabrication in 1997 [9]. However, there are only a few reports focusing on p-type TFTs using CuAlO₂ as channel layers. The primary difficulty is poor crystallinity and impurity phases, such as Cu2O, CuO, Al2O3, and CuAl₂O₄. The first report of a CuAlO₂ TFT was fabricated by magnetron sputtering, and the device exhibits a

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current on/off ratio of 8×10^2 and a hole mobility of 0.97 cm² V⁻¹ s⁻¹ [10]. However, magnetron sputtering needs a strict high vacuum environment and a sophistioperation In cated process. contrast, solution-processed method offers conspicuous advantages, such as simplicity, low-cost, tunable composition, and atmospheric processing. In this work, we present a solution route to prepare CuAlO₂ thin films. The effect of annealing temperature on the microstructure, chemical compositions, morphology, and optical properties of the thin films was investigated systematically. Finally, bottom-gate TFTs using the obtained nanocrystalline CuAlO2 thin films as channel layers were fabricated and they exhibit a mobility of $\sim 0.1 \text{ cm}^2\text{V}^{-1} \text{ s}^{-1}$, a threshold voltage of -1.3 V, and a current on/off ratio of ~ 10 [3].

Methods/Experimental

Precursor Preparation and Thin-Film Fabrication

The CuAlO₂ thin films were prepared by spin coating using copper nitrate trihydrate (Cu(NO₃)₂·3H₂O) and aluminum nitrate nonahydrate (Al(NO₃)₃·9H2O) as starting materials. The molar ratio of two metal salts is 1:1, and the concentration of each salt in ethylene glycol methylether is 0.2 mol/L; acetylacetone was added to form a stable solution in deep green. The entire mixing process was carried out in 80 °C water bath with stirring. Prior to film deposition, the substrates were ultrasonically cleaned with acetone, ethanol, and deionized water for 5 min in each solution. Then, the final precursor was spin-coated with a low rotating speed of 500 rpm for 9 s and followed by a high rotating speed of 5000 rpm for 30 s. After spin-coating, the substrate was annealed at 350 °C for 20 min. The procedures from coating to annealing were repeated four times until the desired thickness (~40 nm) of the films was reached. Finally, the as-deposited films were annealed at 700–1000 °C for 2 h in nitrogen atmosphere and cooled down to room temperature at same atmosphere.

Fabrication of CuAlO₂ TFTs

The CuAlO $_2$ TFTs with a bottom-gate structure were fabricated on SiO $_2$ /Si substrate. Three hundred-nanometer-thick SiO $_2$ serves as the gate dielectric. After CuAlO $_2$ film deposition, 50 nm gold source/drain electrodes were thermal evaporated on the channel layer through a shadow mask. The evaporation rate was 0.08 nm/s, and the channel width (W) and length (L) were 1000 μ m and 100 μ m, respectively. Finally, an indium layer was welded to the Si substrate as the back-gate electrode.

Film and TFT Characterization

The CuAlO₂ film structure was studied by X-ray diffraction (XRD, DX2500) with CuK α radiation (λ =

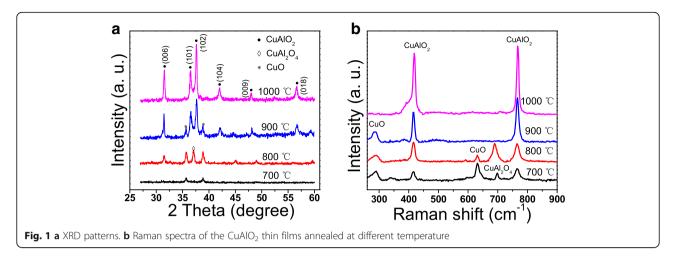
0.154 nm). The Raman spectrum was measured by Renishaw-1000 with a solid-state laser (633 nm). Surface morphologies were measured with scanning electron microscopy (SEM, JSM-5600LV, JEOL) and Veeco Dimension Icon atomic force microscopy (AFM). X-ray photoelectron spectroscopy (XPS) was performed on a Thermo Scientific Escalab 250 Xi spectrometer. XPS spectra were collected after etching the film surface for about 3 nm to minimize surface contamination. The optical transmittance was measured by UV-Vis spectropho-5000). tometer (Varian Cary The electrical characteristics were measured by a semiconductor parameter analyzer (Keithley 2612B).

Results and Discussion

Figure 1a shows the XRD patterns of CuAlO2 thin films annealed at a different temperature. For the film annealed at 700 °C, only weak CuO phase diffraction peaks at 35.8° and 38.9° were observed, indicating that 700 °C is not enough for the formation of CuAlO₂ phase [11]. Two new peaks at 31.7° and 37.1° assigned to CuAlO₂ and CuAl₂O₄ phases, respectively, were observed after 800 °C annealing. When the temperature reached to 900 °C, the intensity of the CuO peaks decrease and the CuAl₂O₄ phase peaks disappear. Several new peaks at 36.8°, 42.5°, 48.5°, 57.5°, and 31.7°, assigned to CuAlO₂ phase, dominated the film [9, 12]. The temperature was further increased to 1000 °C, the peaks intensity increased, and single CuAlO2 phase were obtained. The enhancement of the crystallinity may be attributed to the fact that more energy absorption accelerated the growth of crystallites at higher annealing temperature.

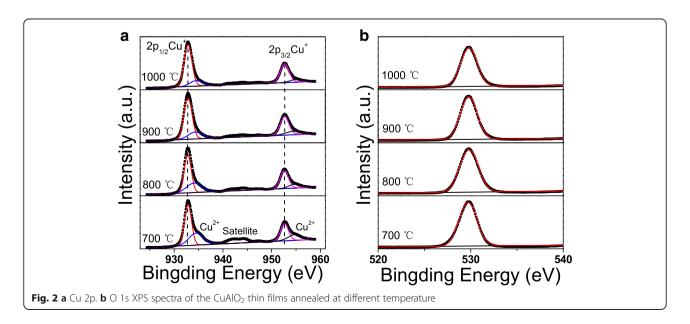
Figure 1b shows the Raman spectra of CuAlO₂ thin films. The four-atom primitive cell of delafossite structure CuAlO₂ leads to 12 normal modes, but only the A_{1g} (416 cm^{-1}) and E_g (771 cm⁻¹) modes are Raman active. As shown in Fig. 1b, it is obvious that two Raman vibration modes, A_{1g} and E_g, both are present for all films [13]. Unlike bulk analysis of XRD, Raman scattering originates from the molecular vibration and lattice vibration that can detect Raman active molecule vibrate from a very small amount of concentration. That explains the existence of CuAlO₂ phase in the 700 °C annealed film, which is not observable in XRD spectrum. Others peaks at 798 cm⁻¹, 297 cm⁻¹, and 632 cm⁻¹ were also observed which are assigned to the F_{2g} mode of CuAl₂O₄, A_g, and Bg modes of CuO, respectively [14]. The peaks of CuO and CuAl₂O₄ phases decrease as the annealing temperature increases from 700 to 1000 °C, and both phases convert to phase CuAlO2 after 1000 °C annealing, which is consistent with XRD results.

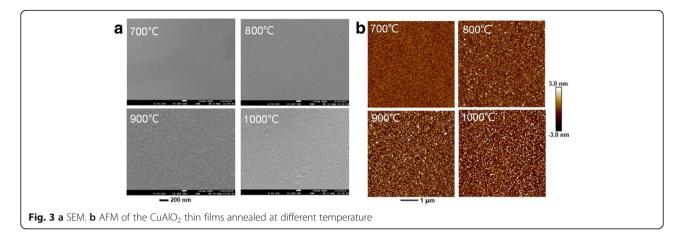
To understand the chemical compositions of CuAlO_2 thin films annealed at different temperature, XPS measurement was carried out and the Cu 2p core levels spectra are shown in Fig. 2a. The typical Cu 2p3/2 peak can



be fitted into two peaks located at ~932.8 and ~ 934.2 eV, which can be attributed to Cu⁺ and Cu²⁺, respectively. Similarly, fitted Cu 2p1/2 deconvolution two peaks are centered at ~952.6 (Cu⁺) and ~954.1 eV (Cu² +), respectively [15]. Since the spin-orbital splitting of Cu 2p is ~ 19.8 eV, the 2p3/2 and 2p1/2 peaks were not constrained for the area ratio during fitting. Nevertheless, the area ratio of the Cu 2p3/2 peak and the Cu 2p1/2 peak is ~ 1.90, being close to the ideal value of 2 determined from electron state densities [14]. The dominated peaks at ~ 932.8 eV (Cu⁺) and ~ 952.6 eV (Cu⁺) indicate that Cu cations mainly exist in Cu+ form in CuAlO₂ lattice. Note that Cu²⁺ state is presented in all films, even no CuO peaks were detected in the high temperature annealed samples by XRD. Meanwhile, the satellite peaks observed from 941.2 to 944.4 eV also implied the presence of CuO. However, satellite peaks are almost negligible after high-temperature annealing, which is consistent with the above XRD observations. Quantitative analysis of the XPS spectra gave $Cu^+/[Cu^++Cu^{2+}]$ atomic ratios of 62.5%, 68.9%, 73.7%, and 78.9% for $CuAlO_2$ thin films annealed at 700, 800, 900, and 1000 °C, respectively, indicating reduction of Cu^{2+} with the increase of annealing temperature [10, 16]. The XPS O 1s peaks are shown in Fig. 2b. It was interesting that the binding energies exhibit symmetrical dominant peaks centered at ~ 529.8 eV, indicating most of oxygen atom are bonded to nearest neighbor metal ions (Cu^+ , Al^{3+} , or Cu^{2+}) in the lattice. It should be noted that the peak at ~ 531.3 eV, attributed to oxygen-related defects, can hardly be distinguished. This result can be explained by the introduction of surface etch process and high crystallization quality.

The surface morphologies of the CuAlO₂ thin films were observed by SEM, as shown in Fig. 3a. All the films exhibit continuous, smooth, and dense structure





morphology without obvious micro-cracks. The grain size is homogeneous and increases with the increase of annealing temperature. The gradually enlarged grain size would lead to the fewer grain boundaries, which act as trapping sites and significantly reduce the mobility for the nanocrystalline CuAlO₂ films [17]. Thus, the CuAlO₂ thin films annealing at high temperature is beneficial to the charge transport and may result high performance TFTs [18]. Surface roughness is another factor which can seriously influence the electrical performance of oxide TFTs [19]. To obtain the root mean square (RMS) roughness, the CuAlO2 thin films were investigated by AFM, as shown in Fig. 3b. The RMS roughness of films annealed at 700 °C, 800 °C, 900 °C, and 1000 °C were 0.92, 1.82, 2.12, and 2.96 nm, respectively. Obviously, the RMS increases with the increase of annealing temperature. Generally, rough surface would result in presence of electrical defects or trapping sites resulting in inferior device performance [20]. Therefore, it was supposed that there should be a competition relation between grain size and surface roughness to affect the performance of nanocrystalline oxide TFTs.

The optical transmission spectra of the CuAlO₂ thin films on fused silica were measured in wavelength range from 200 to 800 nm, as shown in Fig. 4. It was observed that all films have steep absorption edge and strong ultraviolet absorption, which is an indication of the good crystallinity of the films. The average transmittance in the visible light region was calculated from ~60 to ~80%, increasing with the increase of annealing temperature. Tauc's relation $\alpha h \nu = A(h \nu (E_{\sigma})^{1/2}$ is carried out to calculate the optical band gap, where α is the absorption coefficient, A is the constant for a direct transition, h is the Planck's constant, and ν is the photon frequency [21]. The value of Eg is given by the linear extrapolation of the plot of $(\alpha h \nu)^2$ versus $h \nu$ to the energy axis, as shown in the inset of Fig. 4. The E_g were calculated to be 3.25 eV, 3.40 eV, 3.60 eV, and 3.80 eV for the $CuAlO_2$ thin films annealed at 700 °C, 800 °C, 900 °C, and 1000 °C, respectively.

Finally, we fabricated the bottom-gate top-contact TFTs on SiO₂/p-Si substrates to investigate the electrical performance of CuAlO₂ as channel layers. The schematic diagram of device is illustrated in Fig. 5a. The output curves of the CuAlO₂ TFTs at a gate-source voltage $(V_{\rm GS})$ of – 50 V are shown in Fig. 5b. It clearly indicates the on-state current (I_{on}) increases with the increase of annealing temperature. This is mainly attributed to the elimination of insulator-like CuAl₂O₄ phase and the enhancement of nanocrystalline CuAlO2 phase. The transfer curves are shown in Fig. 5c-f, and the CuAlO₂ TFTs exhibit a typical p-type behavior. All the devices show a moderate on/off current ratio $(I_{\rm on}/I_{\rm off})$ of $\sim 10^3$ which perhaps can be further improved by optimizing channel thickness, cation doping, or changing source/drain material [22–24]. The threshold voltage (V_T) is determined as a horizontal axis intercept of a linear fitting to the $I_{\mathrm{DS}}^{-1/2}\text{-}V_{\mathrm{GS}}$ curve. The V_T shift towards the positive with

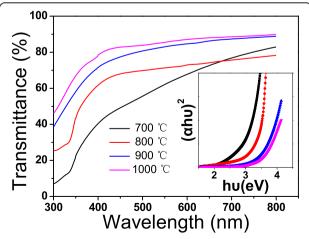


Fig. 4 The optical transmission spectra for $CuAlO_2$ films annealed at different temperature. The inset shows a plot of $(ahv)^2$ vs. hv of the films

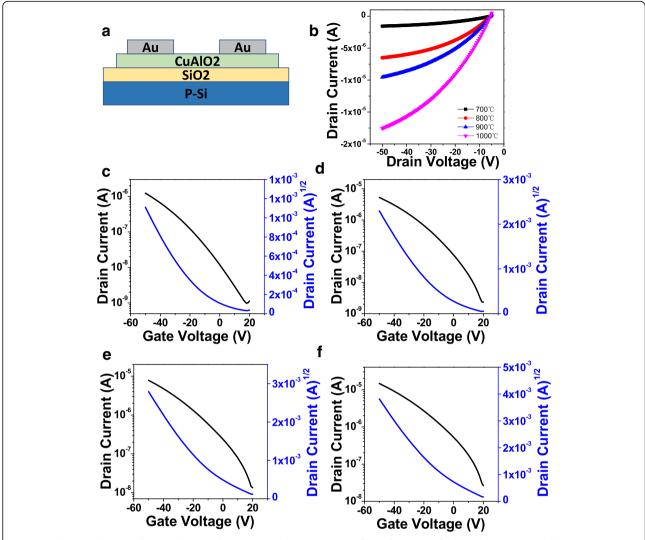


Fig. 5 a Schematic diagram of the CuAlO₂ TFTs. **b** Summarized output curves. **c**–**f** Transfer curves of the CuAlO₂ TFTs annealed at 700 °C, 800 °C, 900 °C, and 1000 °C, respectively

the increase of annealing temperature. The filed effect mobility (μ_{FE}), the subthreshold slope (SS), and the interface trap density (N_t) can be calculated by the following equations [25, 26]:

$$I_{\rm DS} = \frac{1}{2} \mu_{\rm FE} C_{\rm OX} \frac{W}{L} (V_{\rm GS} - V_{\rm T})^2 \tag{1}$$

$$SS = \left(\frac{d\left(\log_{10}I_{DS}\right)}{dV_{GS}}\right)^{-1} \tag{2}$$

$$N_{\rm t} = \left\lceil \frac{\rm SSlog}(e)}{kT/q} - 1 \right\rceil \left(\frac{C_{\rm ox}}{q} \right) \tag{3}$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge of electron, and $C_{\rm ox}$ is the areal capacitance of the gate insulator [27].

The key electrical parameters of the devices are listed in Table 1. It can be seen the SS values, largely higher than reported *n*-type devices, decrease with the increase of annealing temperature, which is consistent with the trend of $V_{\rm T}$. The results can be explained by the reduction of traps at the channel/dielectric interface [28]. The $\mu_{\rm FE}$ values increase from 0.006 to 0.098 $cm^2V^{-1}\ s^{-1}$ as the annealing temperature increased from 700 to 1000 °C, which indicates an improvement of hole transport due to phase conversion from a mixture to nanocrystalline CuAlO₂ and enlargement of grain size. The μ_{FE} are lower than solution-processed CuCrO2 TFTs reported by Nie et al [16]. The reason may be the delafossite nanocrystalline CuAlO₂ structure is lack of Cu-O-Cu lattice content than that of CuCrO₂ [29]. In spite of the annealing temperature of the devices is high for practical applications, this is the first report about solution-processed CuAlO₂ TFTs.

Table 1 Electrical parameters of CuAlO₂ TFTs with different annealing temperature

Annealing temperature (°C)	I_{on} (A)	Mobility (cm 2 V $^{-1}$ s $^{-1}$)	$I_{\rm on}/I_{\rm off}$	V_{T} (V)	SS (V)	$N_{\rm t}$ (10–17 cm ⁻²)
700	1.23×10^{-6}	0.006 ± 0.004	~ 103	-14.7 ± 0.8	14.9	1.79
800	5.27×10^{-6}	0.028 ± 0.008	~ 103	-9.5 ± 0.6	9.1	1.10
900	7.79×10^{-6}	0.051 ± 0.011	~ 103	-2.9 ± 0.5	9.0	1.07
1000	1.45×10^{-5}	0.098 ± 0.009	~ 103	-1.3 ± 0.5	8.6	1.03

Further reduction of the annealing temperature by UV/ ozone photochemical reaction and/or combustion synthesis is now underway [23, 30, 31].

Conclusions

In summary, solution-processed CuAlO₂ thin films were fabricated and annealed in nitrogen atmosphere at different temperature. With the temperature increased from 700 to 1000 °C, the film structure phase transforms from a mixture of CuAl₂O₄ and CuO to nanocrystalline CuAlO₂, as well as the optical transmittance, energy band gap, grain size, and surface roughness of the films increase. The p-type CuAlO2 TFTs performance was strongly dependent on the physical properties and the chemical composition of channel layer. The optimized nanocrystalline CuAlO2 TFT exhibits a threshold voltage of -1.3 V, a mobility of ~ 0.1 cm²V⁻¹ s⁻¹, and a current on/off ratio of $\sim 10^3$. Compared to vacuum-based magnetron sputtering, our work demonstrates a low-cost, solution-processed CuAlO2 TFTs, which represents an important advancement towards the development of complementary metal oxide semiconductor logic circuits.

Abbreviations

AFM: Atomic force microscopy; $C_{\rm ox}$: The areal capacitance of the gate insulator; $l_{\rm on}/l_{\rm off}$: On/off current ratio; k: The Boltzmann constant; L: The channel length; $N_{\rm c}$: The interface trap density; q: The elementary charge of electron; SEM: Scanning electron microscopy; SS: The subthreshold slope; T: The absolute temperature; TFTs: Thin-film transistors; $V_{\rm T}$: Threshold voltage; W: The channel width; XPS: X-ray photoelectron spectroscopy; XRD: X-ray diffraction; $\mu_{\rm FE}$: Filed effect mobility

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Availability of Data and Materials

Presented in the main paper.

Authors' Contributions

SL carried out the main part of the experiments and drafted the manuscript. XZ designed the experiment and polished the manuscript. PZ participated in the measurements and performed the analysis. XS and HZ participated in the design of the study. WZ gave suggestions on the experimental design and polished the manuscript. All authors read and approved the final manuscript.

Competing Interests

The authors declare that they have no competing interests.

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